

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

1-30. (Canceled)

1 31. (Currently amended): A memory access method in a data processing unit
2 comprising dynamic memory and re-programmable non-volatile memory, the method
3 comprising:

4 detecting a write operation to an area in the re-programmable non-volatile
5 memory;

6 determining a caching location which identifies an area of memory in ~~a~~the
7 dynamic memory to which data to be written by the write operation can be cached, the area of
8 memory identified by the caching location referred to as a caching area; and

9 writing the data to the caching area instead of writing the data to the area in the
10 re-programmable non-volatile memory,

11 wherein the caching area is associated with the area in the re-programmable non-
12 volatile memory.

1 32. (Currently amended): The method of claim 31 wherein the step of
2 determining a caching location comprises:

3 determining if ~~the data can be stored in the dynamic memory~~ has capacity to store
4 the data, and if not then:

5 identifying one or more memory locations in the dynamic memory; and
6 writing content in the one or more memory locations to the re-
7 programmable non-volatile memory; and

8 providing an address in the dynamic memory as the caching location in the area of
9 memory.

1 33. (Original): The method of claim 32 wherein the step of determining a
2 caching location in the dynamic memory is limited to determining a caching location in a
3 segment of the dynamic memory.

1 34. (Original): The method of claim 31 further including detecting a second
2 write operation to the area in the re-programmable non-volatile memory and writing the data
3 associated with the second write operation to the area of memory identified by the caching
4 location instead of writing the data to the area in the re-programmable non-volatile memory.

1 35. (Original): The method of claim 31 further including detecting a second
2 write operation to a second area in the re-programmable non-volatile memory, determining if
3 there is a caching area in the dynamic memory that is associated with the second area and if there
4 is then writing data associated with the second write operation to the caching area associated
5 with the second area.

1 36. (Original): The method of claim 31 wherein an address space of the re-
2 programmable non-volatile memory is equal to or greater than an address space of the dynamic
3 memory.

1 37. (Original): The method of claim 32 wherein the step of identifying one or
2 more memory locations is based on the size of the data.

1 38. (Original): The method of claim 32 wherein the step of identifying one or
2 more memory locations is based on contents of the data.

1 39. (Original): The method of claim 38 wherein the step of identifying one or
2 more memory locations includes applying a hash function on the data to produce a hash result,
3 the one or more locations determined based on the hash result.

1 40. (Currently amended): The method of claim 31 wherein the re-
2 programmable non-volatile memory is one of an EEPROM (electrically erasable programmable
3 read-only memory) and/or a flash memory.

1 41. (Original): The method of claim 31 further including obtaining an address
2 range which defines the area of memory in the dynamic memory.

1 42. (Original): The method of claim 31 further including detecting a read
2 operation from the re-programmable non-volatile memory and reading the re-programmable non-
3 volatile memory to effect the read operation.

1 43. (Original): The method of claim 31 further including detecting a read
2 operation from the re-programmable non-volatile memory and reading one or more memory
3 locations from the area of memory in the dynamic memory to effect the read operation.

1 44. (Currently amended): A data processing unit comprising:
2 a dynamic memory;
3 a memory bus for accessing a-the dynamic memory;
4 a re-programmable non-volatile memory;
5 memory access logic operatively coupled to the memory bus and to the re-
6 programmable non-volatile memory; and

7 processor logic operatively coupled to the memory access logic to transfer data
8 with the dynamic memory via the memory bus and to transfer data with the re-programmable
9 non-volatile memory,

10 the memory access logic configured to detect a write operation to the re-
11 programmable non-volatile memory,

12 the processor logic configured to respond to the memory access logic detecting
13 the write operation and to:

14 identify a caching location in ~~the area of~~an area of the dynamic memory
15 wherein data to be written by the write operation can be cached; and

16 store the data in the area of the dynamic memory identified by the caching
17 location.

1 45. (Currently amended): The data processing unit of claim 44 wherein the
2 ~~memory accessprocessor~~ logic is further configured to:

3 determine if ~~the data can be stored in the area of the dynamic memory has~~
4 capacity to store the data; and

5 provide an address in the area of the dynamic memory as the caching location in
6 ~~the area of memory~~,

7 wherein if it is determined that the caching location lacks capacity to store the
8 ~~data~~data cannot be stored in the area of memory, then:

9 identify one or more other memory locations in the area of the dynamic
10 memory; and

11 write content in the one or more other memory locations to the re-
12 programmable non-volatile memory,

13 wherein the one or more other memory locations are-become available for caching
14 a write operation.

1 46. (Original): The data processing unit of claim 44 wherein an address space
2 of the re-programmable non-volatile memory is equal to or greater than an address space of the
3 dynamic memory.

1 47. (Currently amended): The data processing unit of claim 44 wherein the
2 re-programmable non-volatile memory is one of an EEPROM (electrically erasable
3 programmable read-only memory) and-or a flash memory.

1 48. (Original): The data processing unit of claim 44 wherein the dynamic
2 memory is a random access memory.

1 49. (Original): The data processing unit of claim 44 wherein the memory
2 access logic is further configured to detect a read operation from the re-programmable non-
3 volatile memory and to effect a read operation therefrom.

1 50. (Original): The data processing unit of claim 44 wherein the memory
2 access logic is further configured to detect a read operation from the re-programmable non-
3 volatile memory and to access the area in memory in the dynamic memory to effect the read
4 operation.

1 51. (Original): A memory access method comprising:
2 detecting a write operation to a re-programmable non-volatile memory; and
3 if a destination address associated with the write operation is within a first range
4 of addresses, then performing a fast write operation of data associated with the write operation to
5 the re-programmable non-volatile memory.

1 52. (Original): The method of claim 51 wherein the first range of addresses
2 spans the entire address space of the re-programmable non-volatile memory.

1 53. (Original): The method of claim 51 wherein if the destination address is
2 not within the first range of addresses, then performing a slow write operation of the data to the
3 re-programmable non-volatile memory.

1 54. (Original): The method of claim 51 wherein the first range of addresses
2 spans a range of addresses less than the address space of the re-programmable non-volatile
3 memory.

1 55. (Original): The method of claim 51 wherein the step of performing a fast
2 write operation is performed if the destination address falls within any of a plurality of ranges of
3 addresses.

1 56. (Original): A memory access method comprising:
2 detecting a write operation to a non-volatile memory;
3 determining an access mode;
4 if the access mode is a first mode, then performing a fast write operation of data
5 associated with the write operation to the non-volatile memory;
6 if the access mode is a second mode, then performing a slow write operation of
7 the data associated with the write operation; and
8 if the access mode is a third mode, then:
9 if the destination address associated with the write operation is within a
10 first range of addresses, then performing a fast write operation of the data associated with
11 the write operation to the non-volatile memory;
12 if the destination address is not within the first range of addresses, then
13 performing a slow write operation of the data to the non-volatile memory; and
14 if the access mode is a fourth mode, then:
15 determining a caching location which identifies an area of memory in a
16 dynamic memory to which data to be written by the write operation can be cached, the
17 area of memory identified by the caching location referred to as a caching area; and
18 writing the data to the caching area instead of writing the data to the area
19 in the non-volatile memory,
20 wherein the caching area is associated with the area in the non-volatile
21 memory.

1 57-62.. (Canceled)

1 63. (Original): A memory access method for accessing a re-programmable
2 non-volatile memory comprising:

3 detecting a write operation to the re-programmable non-volatile memory, the
4 write operation having an associated destination address and associated one or more data to be
5 written to the re-programmable non-volatile memory;

6 determining an operating mode;

7 if the operating mode indicates a first mode of operation, then:

8 performing a partial write operation of each datum to the re-programmable
9 non-volatile memory, if the destination address is within a first range of addresses; and

10 performing a full write operation of each datum to the re-programmable
11 non-volatile memory, otherwise;

12 if the operating mode indicates a second mode of operation, then performing a full
13 write operation of each datum to the re-programmable non-volatile memory;

14 if the operating mode indicates a third mode of operation, then performing a
15 partial write operation of each datum to the re-programmable non-volatile memory; and

16 if the operating mode indicates a fourth mode of operation, then:

17 determining a caching location which identifies an area of memory in a
18 dynamic memory where the data can be cached; and

19 writing the data in the area of memory identified by the caching location
20 instead of writing to the re-programmable non-volatile memory.

1 64. (Currently amended): The method of claim 63 wherein the re-
2 programmable non-volatile memory is one of an EEPROM (electrically erasable programmable
3 read-only memory) and-or a flash memory.